STIC Search Report
EIC 2800

STIC Database Tracking Number: 202235

TO:	From:
Dung Le **Location: JEF 6C89** **Art Unit: 2818** **Thursday, September 21, 2006** **Case Serial Number: 10/600039**	**Mary S. Mims** **Location: STIC-EIC2800** **JEF-4B59** **Phone: 25928** **Email: Mary.Mims@USPTO.GOV**

Search Notes

Examiner Dung Le,

Please find attached results of your search for 10/600039. The search was conducted using databases on STN related to interconnect. The tagged documents appear to be the closest documents located during our search. Please review all of the results.

Based on this, if you have questions or would like a refocused search, please contact me.

Thanks

Mary S. Mims

Mary S. Mims

Jackson, Diane 207235

From: DUNG LE [dunganh.le@uspto.gov]
Sent: Wednesday, September 20, 2006 7:39 AM
To: STIC-EIC2800
Subject: Database Search Request, Serial Number: 10/600039

Requester:
DUNG LE (P/2818)
Art Unit:
GROUP ART UNIT 2818
Employee Number:
77672
Office Location:
JEF 06C89
Phone Number:
(571)272-1784
Mailbox Number:
Jef 6D85

SEP 20 RECD

Case serial number:
10/600039
Class / Subclass(es):
438/627,643,653
Earliest Priority Filing Date:
4/1/2001
Format preferred for results:
Paper
Search Topic Information:
a) Ru as a diffusion barrier for copper.
b) RuO2 as a diffusion barrier for copper.
c) Ru and RuO2 as a diffusion barrier for copper.
(Ru: Ruhthenium; RuO2: Ruthenium oxide).

Thanks and have a nice day.
Special Instructions and Other Comments:
I summitted one earlier with invalid earliest priority filling date.
Valid earliest priority filling date: 4/1/2001.

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     (FILE 'HOME' ENTERED AT 14:38:08 ON 21 SEP 2006)

     FILE 'CAPLUS' ENTERED AT 14:38:39 ON 21 SEP 2006
L1             1 SEA ABB=ON  PLU=ON  US20040051117/PN
                 SEL RN
L2        567480 SEA ABB=ON  PLU=ON  (11113-84-1/BI OR 12030-49-8/BI OR
                 12036-10-1/BI OR 12645-46-4/BI OR 7439-88-5/BI OR 7440-18-8/BI
                 OR 7440-50-8/BI)
L3             1 SEA ABB=ON  PLU=ON  L1 AND L2
                 D IBIB ABS HITSTR HITIND

     FILE 'REGISTRY' ENTERED AT 14:44:02 ON 21 SEP 2006
L4            28 SEA ABB=ON  PLU=ON  O.RU/MF
L5           148 SEA ABB=ON  PLU=ON  O RU/ELF
L6        150050 SEA ABB=ON  PLU=ON  RU/ELS

     FILE 'CAPLUS' ENTERED AT 14:44:56 ON 21 SEP 2006
L7         98839 SEA ABB=ON  PLU=ON  (L4 OR L5 OR L6)
L8       1351166 SEA ABB=ON  PLU=ON  INTERCONNECT OR DAMASCENE OR IC OR
                 INTEGRAT? CIRCUIT? OR SEMICONDUCT? OR VIA
L9         10613 SEA ABB=ON  PLU=ON  L7 AND L8
L10      3616199 SEA ABB=ON  PLU=ON  BARRIER OR COAT? OR LAYER? OR DIFFUS? OR
                 PROTECT? OR IMPED?
L11         3344 SEA ABB=ON  PLU=ON  L9 AND L10
L12      1186512 SEA ABB=ON  PLU=ON  COPPER OR CU OR 7440-88-5/RN
L13          830 SEA ABB=ON  PLU=ON  L11 AND L12

     FILE 'REGISTRY' ENTERED AT 14:56:40 ON 21 SEP 2006
L14            1 SEA ABB=ON  PLU=ON  7440-50-8/RN

     FILE 'CAPLUS' ENTERED AT 14:56:41 ON 21 SEP 2006
L15        518525 SEA ABB=ON  PLU=ON  L14
L16           652 SEA ABB=ON  PLU=ON  L13 AND L15
L17         15447 SEA ABB=ON  PLU=ON  DIFFUS?(2W)BARRIER
L18           120 SEA ABB=ON  PLU=ON  L16 AND L17
L19           137 SEA ABB=ON  PLU=ON  L17(L)L7
L20            29 SEA ABB=ON  PLU=ON  L18 AND L19
                 D IBIB ABS HITSTR HITIND 1-29
L21           120 SEA ABB=ON  PLU=ON  L18 AND PY>=2001
L22           112 SEA ABB=ON  PLU=ON  L18 AND PY>=2002
L23             3 SEA ABB=ON  PLU=ON  L18 NOT (L22 OR L20)
                 D IBIB ABS HITSTR 1-3

     FILE 'INSPEC, COMPENDEX' ENTERED AT 15:38:35 ON 21 SEP 2006

L24         21134 SEA ABB=ON  PLU=ON  (RUO2 OR RU)/ET
L25        270908 SEA ABB=ON  PLU=ON  CU/ET
L26       1825792 SEA ABB=ON  PLU=ON  L8
L27          9513 SEA ABB=ON  PLU=ON  L17
L28            20 SEA ABB=ON  PLU=ON  L24 AND L25 AND L26 AND L27
L29            18 DUP REM L28 (2 DUPLICATES REMOVED)
                 D IALL 1-18
L30       2371021 SEA ABB=ON  PLU=ON  L10
L31           130 SEA ABB=ON  PLU=ON  L24 AND L25 AND L26 AND L30
L32            82 SEA ABB=ON  PLU=ON  L31 AND PY>=2001
L33            48 SEA ABB=ON  PLU=ON  L31 NOT (L32 OR L29)
                 D IALL 1-48
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09/21/2006 10/600039 Le

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     FILE 'JAPIO, KOREAPAT' ENTERED AT 15:53:55 ON 21 SEP 2006
L34       929651 SEA ABB=ON  PLU=ON  L8

L35      1395103 SEA ABB=ON  PLU=ON  L10
L36         7742 SEA ABB=ON  PLU=ON  RUTHENIUM OR RU
L37       125399 SEA ABB=ON  PLU=ON  CU OR COPPER
L38           61 SEA ABB=ON  PLU=ON  L34 AND L35 AND L36 AND L37
L39           61 DUP REM L38 (0 DUPLICATES REMOVED)
L40           22 SEA ABB=ON  PLU=ON  L39 AND PY>=2001
L41           39 SEA ABB=ON  PLU=ON  L39 NOT L40
                 D IALL 1-39
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L20 ANSWER 29 OF 29 CAPLUS COPYRIGHT 2006 ACS on STN
ACCESSION NUMBER: 1999:262008 CAPLUS
DOCUMENT NUMBER: 130:319462
TITLE: **Diffusion barrier layer** of **semiconductor** device and its production method
INVENTOR(S): Horii, Hideki; Hwang, Chul-Sung
PATENT ASSIGNEE(S): Samsung Electronics Co., Ltd., S. Korea
SOURCE: Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DOCUMENT TYPE: Patent
LANGUAGE: Japanese
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 11111919	A2	19990423	JP 1998-160154	19980609
TW 451389	B	20010821	TW 1998-87106111	19980421
US 6177284	B1	20010123	US 1998-156723	19980918
PRIORITY APPLN. INFO.:			KR 1997-49759 A	19970929

AB A reliable **semiconductor** device comprises a **diffusion barrier layer** containing a Group VB or VIB metal such as Ta, Al, and N between conductor **layers**. Addnl., the **barrier layer** may contain oxygen. Specifically, the conductor **layer** may comprise a capacitor electrode such as Pt, Rh, Ru, Ir, Os, Pd, PtOx, RhOx, IrOx, RuOx, OsOx, PdOx, CaRuO3, SrRuO3, CaIrO3, SrIrO3, **Cu**, Al, Ta, WSix, Mo, MoSix, W, Au, TiN, and/or TaN. The fabrication steps for the above device are also described.

IT **7440-18-8**, Ruthenium, processes **7440-50-8**, **Copper**, processes **12169-14-1**, Ruthenium strontium oxide (RuSrO3) **12313-89-2**, Calcium ruthenium oxide (CaRuO3)
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**diffusion barrier layer** for **semiconductor** device having conductor **layers** of)

RN 7440-18-8 CAPLUS
CN Ruthenium (8CI, 9CI) (CA INDEX NAME)

Ru

RN 7440-50-8 CAPLUS
CN Copper (7CI, 8CI, 9CI) (CA INDEX NAME)

Cu

RN 12169-14-1 CAPLUS
CN Ruthenium strontium oxide (RuSrO3) (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number
O	3	17778-80-2
Sr	1	7440-24-6

Ru	1	7440-18-8

RN 12313-89-2 CAPLUS
CN Calcium ruthenium oxide (CaRuO3) (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number
O	3	17778-80-2
Ca	1	7440-70-2
Ru	1	7440-18-8

IC ICM H01L027-04
ICS H01L021-822
CC 76-3 (Electric Phenomena)
ST **diffusion barrier** capacitor electrode **semiconductor** device fabrication
IT Capacitor electrodes
Diffusion barrier
Semiconductor devices
(**diffusion barrier layer** for conductor **layers** of **semiconductor** device)
IT **Semiconductor** device fabrication
(formation of **diffusion barrier layer** for conductor **layers** in)
IT 53322-74-0, Aluminum tantalum nitride 157781-72-1, Aluminum nitrogen tantalum oxide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**diffusion barrier layer** for conductor **layers** of **semiconductor** device)
IT 7429-90-5, Aluminum, processes 7439-88-5, Iridium, processes 7439-98-7, Molybdenum, processes 7440-04-2, Osmium, processes 7440-05-3, Palladium, processes 7440-06-4, Platinum, processes 7440-16-6, Rhodium, processes **7440-18-8**, Ruthenium, processes 7440-25-7, Tantalum, processes 7440-33-7, Tungsten, processes **7440-50-8**, **Copper**, processes 7440-57-5, Gold, processes 11104-85-1, Molybdenum silicide 11113-77-2, Palladium oxide 11113-84-1, Ruthenium oxide 11129-89-8, Platinum oxide 12013-42-2, Calcium iridium oxide (CaIrO3) 12033-62-4, Tantalum nitride (TaN) **12169-14-1**, Ruthenium strontium oxide (RuSrO3) 12196-57-5, Iridium strontium oxide (IrSrO3) **12313-89-2**, Calcium ruthenium oxide (CaRuO3) 12627-41-7, Tungsten silicide 12645-46-4, Iridium oxide 12680-36-3, Rhodium oxide 25583-20-4, Titanium nitride (TiN) 61970-39-6, Osmium oxide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**diffusion barrier layer** for **semiconductor** device having conductor **layers** of)

L20 ANSWER 27 OF 29 CAPLUS COPYRIGHT 2006 ACS on STN
ACCESSION NUMBER: 2001:844958 CAPLUS
DOCUMENT NUMBER: 135:379634
TITLE: **Diffusion barriers** between noble metal electrodes and metalization **layers**, and **integrated circuit** and **semiconductor** devices comprising same
INVENTOR(S): Kirlin, Peter S.; Summerfelt, Scott R.; Mcintryre, Paul
PATENT ASSIGNEE(S): Advanced Technology Materials, Inc., USA
SOURCE: U.S., 19 pp.
CODEN: USXXAM
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6320213	B1	20011120	US 1997-994089	19971219
PRIORITY APPLN. INFO.:			US 1997-994089	19971219

AB A dynamic random access memory device includes storage capacitors using a high dielec. constant material, such as, BaSrTiO3, SrBi2Ta2O9, and PbZrTiO3, for the capacitors' insulator. The device includes a conductive plug formed over and connecting with a **semiconductor** substrate. A buffer **layer** of Ti silicide lays over the plug, and this **layer** serves to trap dangling bonds and to passivate the underlying surface. A 1st **diffusion barrier layer**, e.g., Ti Al nitride, covers the Ti silicide. A capacitor 1st electrode lays over the **diffusion barrier layer**. The high dielec. constant material is laid over the capacitor 1st electrode. A capacitor 2nd electrode is laid over the high dielec. constant material. A 2nd **diffusion barrier layer** is deposited on the capacitor 2nd electrode. A conductor, such as Al, is laid over the 2nd **diffusion barrier layer**. An isolation dielec. can be deposited over the conductor at a high temperature without causing O or metallic **diffusion** through the 1st and 2nd **diffusion barrier layers**.

IT **7440-18-8**, Ruthenium, uses **7440-50-8**, **Copper**, uses
RL: DEV (Device component use); USES (Uses)
(capacitor electrode material; **diffusion barriers** between noble metal electrodes and metalization **layers**, and **integrated circuit** and **semiconductor** devices comprising same)
RN 7440-18-8 CAPLUS
CN Ruthenium (8CI, 9CI) (CA INDEX NAME)

Ru

RN 7440-50-8 CAPLUS
CN Copper (7CI, 8CI, 9CI) (CA INDEX NAME)

Cu

IT **187749-47-9**, Ruthenium silicon oxide **256943-05-2**, Ruthenium nitride silicide
RL: DEV (Device component use); USES (Uses)
(**diffusion barrier** material; **diffusion barriers** between noble metal electrodes and metalization **layers**, and **integrated circuit** and **semiconductor** devices comprising same)
RN 187749-47-9 CAPLUS
CN Ruthenium silicon oxide (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number
O	x	17778-80-2
Si	x	7440-21-3
Ru	x	7440-18-8

RN 256943-05-2 CAPLUS
CN Ruthenium nitride silicide (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number
N	x	17778-88-0
Si	x	7440-21-3
Ru	x	7440-18-8

IC ICM H01L029-76
ICS H01L029-94; H01L031-062; H01L031-113
INCL 257295000
CC 76-3 (Electric Phenomena)
ST **semiconductor** device fabrication **diffusion barrier** noble metal electrode metalization; dynamic RAM **semiconductor** device storage capacitor
IT Memory devices
(DRAM (dynamic random access); **diffusion barriers** between noble metal electrodes and metalization **layers**, and **integrated circuit** and **semiconductor** devices comprising same)
IT Capacitor electrodes
Capacitors
Dielectric films
Diffusion barrier
Integrated circuits
Passivation
Semiconductor device fabrication
(**diffusion barriers** between noble metal electrodes and metalization **layers**, and **integrated circuit** and **semiconductor** devices comprising same)
IT Electric contacts
(plugs; **diffusion barriers** between noble metal electrodes and metalization **layers**, and **integrated circuit** and **semiconductor** devices comprising same)
IT Rare earth pnictides
RL: DEV (Device component use); USES (Uses)
(rare earth nitrides, **diffusion barrier** material; **diffusion barriers** between noble metal electrodes and metalization **layers**, and **integrated circuit** and **semiconductor** devices comprising same)

IT 7429-90-5, Aluminum, uses 7439-88-5, Iridium, uses 7440-05-3, Palladium, uses 7440-06-4, Platinum, uses 7440-15-5, Rhenium, uses 7440-16-6, Rhodium, uses **7440-18-8**, Ruthenium, uses 7440-21-3, Silicon, uses 7440-22-4, Silver, uses **7440-50-8**, **Copper**, uses 7440-56-4, Germanium, uses 7440-57-5, Gold, uses
RL: DEV (Device component use); USES (Uses)
(capacitor electrode material; **diffusion barriers** between noble metal electrodes and metalization **layers**, and **integrated circuit** and **semiconductor** devices comprising same)

IT 12738-91-9, Titanium silicide
RL: DEV (Device component use); USES (Uses)
(device buffer **layer**; **diffusion barriers** between noble metal electrodes and metalization **layers**, and **integrated circuit** and **semiconductor** devices comprising same)

IT 1314-36-9, Yttrium oxide, uses 1314-61-0, Tantalum pentoxide 11115-71-2, Bismuth titanate 12030-85-2, Niobium potassium oxide (NbKO3) 12030-91-0, Potassium tantalum oxide (KTaO3) 12326-05-5, Lead niobate (PbNbO3) 12676-60-7, Lanthanum lead titanium zirconium oxide (La0-1Pb0-1Ti0-1Zr0-1O3) 37307-70-3, Lead zinc niobate 37349-19-2, Lead magnesium niobate 50811-07-9, Bismuth strontium tantalum oxide (Bi2SrTa2O9) 122989-95-1, Lead scandium tantalum oxide 374594-15-7
RL: DEV (Device component use); USES (Uses)
(device dielec. film; **diffusion barriers** between noble metal electrodes and metalization **layers**, and **integrated circuit** and **semiconductor** devices comprising same)

IT 7440-02-0, Nickel, uses 7440-25-7, Tantalum, uses 7440-32-6, Titanium, uses 7440-33-7, Tungsten, uses 7440-48-4, Cobalt, uses 7440-55-3, Gallium, uses 11074-66-1, Strontium nitride (SrN) 12370-86-4, Calcium nitride (CaN) 24304-00-5, Aluminum nitride (AlN) 25764-10-7, Lanthanum nitride (LaN) 25764-12-9, Scandium nitride (ScN) 25764-13-0, Yttrium nitride (YN) 25817-87-2, Hafnium nitride (HfN) 58984-34-2, Aluminum rhodium oxide 60195-15-5, Magnesium nitride (MgN) 91914-87-3, Titanium boride nitride (TiBN) 148793-50-4, Aluminum titanium nitride (AlTiN) 155184-14-8, Aluminum palladium oxide 160277-12-3, Tantalum boride nitride 164144-82-5, Platinum nitride silicide 164144-84-7, Palladium nitride silicide 167493-27-8, Titanium nitride silicide (TiNSi) 173958-73-1, Silver nitride silicide 175295-30-4, Barium nitride 176660-45-0, Tantalum nitride silicide (TaNSi) **187749-47-9**, Ruthenium silicon oxide 188876-71-3, Aluminum palladium nitride 188876-77-9, Iridium silicon oxide 188876-79-1, Rhenium nitride silicide 188876-81-5, Gold nitride silicide 195978-17-7, Platinum silicon oxide 251092-01-0, Palladium silicon oxide **256943-05-2**, Ruthenium nitride silicide 256943-08-5, Iridium nitride silicide 374594-12-4, Boron palladium oxide 374594-13-5, Palladium boride nitride 374594-14-6, Rhenium silicon oxide
RL: DEV (Device component use); USES (Uses)
(**diffusion barrier** material; **diffusion barriers** between noble metal electrodes and metalization **layers**, and **integrated circuit** and **semiconductor** devices comprising same)

REFERENCE COUNT: 19 THERE ARE 19 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

L23 ANSWER 1 OF 3 CAPLUS COPYRIGHT 2006 ACS on STN
ACCESSION NUMBER: 2001:863478 CAPLUS
DOCUMENT NUMBER: 135:379757
TITLE: Method for self-aligned formation of silicide contacts using metal silicon alloys for limited silicon consumption and for reduction of bridging
INVENTOR(S): Brodsky, Stephen Bruce; Cabral, Cyril, Jr.; Carruthers, Roy Arthur; Harper, James Mckell Edwin; Lavoie, Christian; O'neil, Patricia Ann; Wang, Yun Yu
PATENT ASSIGNEE(S): International Business Machines Corporation, USA
SOURCE: U.S., 9 pp.
CODEN: USXXAM
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6323130	B1	20011127	US 2000-515033	20000306
PRIORITY APPLN. INFO.:			US 2000-515033	20000306

AB A method of substantially reducing Si consumption and bridging during metal silicide contact formation comprising the steps of: (a) forming a metal silicon alloy **layer** over a silicon-containing substrate containing an electronic device to be elec. contacted, said silicon in said alloy **layer** being .ltorsim.30 at and said metal is Co, Ni or mixts. thereof; (b) annealing said metal silicon alloy **layer** at a temperature of from .apprx.300° to .apprx.500°. so as to form a metal rich silicide **layer** that is substantially nonetchable compared to said metal silicon alloy or pure metal; (c) selectively removing any nonreacted metal silicon alloy over nonsilicon regions; and (d) annealing said metal rich silicide **layer** under conditions effective in forming a metal silicide phase that is in its lowest resistance phase. An optional oxygen **barrier layer** may be formed over the metal silicon alloy **layer** prior to annealing step (b).

IT **7440-18-8**, Ruthenium, uses **7440-50-8**, **Copper**, uses
RL: MOA (Modifier or additive use); USES (Uses)
(metallic additives in self-aligned formation of silicide contacts using metal silicon alloys for limited silicon consumption and for reduction of bridging)

RN 7440-18-8 CAPLUS
CN Ruthenium (8CI, 9CI) (CA INDEX NAME)

Ru

RN 7440-50-8 CAPLUS
CN Copper (7CI, 8CI, 9CI) (CA INDEX NAME)

Cu

REFERENCE COUNT: 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

L23 ANSWER 2 OF 3 CAPLUS COPYRIGHT 2006 ACS on STN
ACCESSION NUMBER: 2001:480743 CAPLUS
DOCUMENT NUMBER: 135:69614
TITLE: Separately optimized gate structures for n-channel and p-channel transistors in an **integrated circuit** fabrication
INVENTOR(S): Gardner, Mark I.; Fulford, H. Jim, Jr.
PATENT ASSIGNEE(S): Advanced Micro Devices, Inc., USA
SOURCE: U.S., 15 pp.
CODEN: USXXAM
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6255698	B1	20010703	US 1999-301263	19990428
PRIORITY APPLN. INFO.:			US 1999-301263	19990428

AB An **integrated circuit** containing sep. optimized gate structures for n-channel and p-channel transistors is provided and formed. Original gate structures for both n-channel and p-channel transistors are patterned over appropriately-doped active regions of a **semiconductor** substrate. **Protective** dielecs. are formed over the **semiconductor** substrate to the same elevation level as the upper surfaces of the original gate structures, so that only the upper surfaces of the gate structures are exposed. A masking **layer** was used to cover the gate structures of either the p-channel or the n-channel transistors. The uncovered gate structures are removed, forming a trench within the **protective** dielec. in place of each removed gate structure. The trenches are refilled with a new gate structure which is preferably optimized for operation of the appropriate transistor type (n-channel or p-channel).

IT **7440-18-8**, Ruthenium, processes **7440-50-8**, **Copper**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(sep. optimized gate structures for n-channel and p-channel transistors in **integrated circuit** fabrication using)
RN 7440-18-8 CAPLUS
CN Ruthenium (8CI, 9CI) (CA INDEX NAME)

Ru

RN 7440-50-8 CAPLUS
CN Copper (7CI, 8CI, 9CI) (CA INDEX NAME)

Cu

REFERENCE COUNT: 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

L23 ANSWER 3 OF 3 CAPLUS COPYRIGHT 2006 ACS on STN
ACCESSION NUMBER: 2001:221984 CAPLUS
DOCUMENT NUMBER: 134:230739
TITLE: Fabricating **integrated circuit interconnects**
INVENTOR(S): Mucha, John Aaron
PATENT ASSIGNEE(S): Lucent Technologies, Inc., USA
SOURCE: U.S., 9 pp.
CODEN: USXXAM
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6207570	B1	20010327	US 1999-378250	19990820

PRIORITY APPLN. INFO.: US 1999-378250 19990820

AB A method for manufacturing **integrated circuits**; particularly, (1) a method for removing **barrier** material that lies between **Cu** conductors in **damascene** interconnections, and (2) a method for removing a thin **layer** of Si nitride material that was intentionally un-etched during the formation of trenches and **vias** in **damascene interconnect** dielec. and thereby not exposing **Cu** metal.

IT **7440-18-8**, Ruthenium, processes **7440-50-8**, **Copper**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in fabricating **integrated circuit interconnects**)

RN 7440-18-8 CAPLUS
CN Ruthenium (8CI, 9CI) (CA INDEX NAME)

Ru

RN 7440-50-8 CAPLUS
CN Copper (7CI, 8CI, 9CI) (CA INDEX NAME)

Cu

REFERENCE COUNT: 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD. ALL CITATIONS AVAILABLE IN THE RE FORMAT

L41 ANSWER 1 OF 39 JAPIO (C) 2006 JPO on STN
ACCESSION NUMBER: 2000-269455 JAPIO
TITLE: **SEMICONDUCTOR** DEVICE AND ITS MANUFACTURE
INVENTOR: KUMAGAI YUKIHIRO; MIURA HIDEO; OTA HIROYUKI; IWASAKI TOMIO; ASANO ISAMU
PATENT ASSIGNEE(S): HITACHI LTD
PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 2000269455	A	20000929	Heisei	H01L027-108

APPLICATION INFORMATION
STN FORMAT: JP 1999-67840 19990315
ORIGINAL: JP11067840 Heisei
PRIORITY APPLN. INFO.: JP 1999-67840 19990315
SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
INT. PATENT CLASSIF.:
MAIN: H01L027-108
SECONDARY: H01L021-8242; H01L021-3205; H01L027-10; H01L021-8247; H01L029-788; H01L029-792

ABSTRACT:
PROBLEM TO BE SOLVED: To realize a low contact resistance without reducing function to improve resistance to migration and reliability, by using the same material Ru, Pt, or Ir for the **barrier** metal of an upper electrode and a wiring.
SOLUTION: A transistor formed on a silicon substrate 1 is constituted by a gate oxide film 2, a gate electrode 3, and a **diffusion layer**. A silicon oxide film 5 is formed on the top and the side wall of the gate oxide film 2, a bit line 7 is connected to the silicon oxide film 5 **via** a contact plug 6 and the whole top surface of them is covered with an interlayer insulating film 8. A storage capacitor 10 is formed **via** a contact plug 4, the top surface of the storage capacitor 10 is covered with an interlayer insulating film 25 and the portion other than the top surface is covered with the interlayer insulating film 8. A plug 21 covered with **barrier** metals 23a, 23b is formed in a contact hole and is connected to the upper electrode 13 of the storage capacitor 10, a wiring 22 covered with **barrier** metals 24a, 24b is formed, and the plug 21 and the wiring 22 is made of **Cu** or a **Cu** alloy and covered with a **protective** film 27. Therefore, this can improve the reliability of a **semiconductor** device and reduce its material cost.

L41 ANSWER 2 OF 39 JAPIO (C) 2006 JPO on STN
ACCESSION NUMBER: 2000-208511 JAPIO
TITLE: **SEMICONDUCTOR** DEVICE
INVENTOR: IWASAKI TOMIO; MIURA HIDEO; ASANO ISAMU
PATENT ASSIGNEE(S): HITACHI LTD
PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 2000208511	A	20000728	Heisei	H01L021-3205

APPLICATION INFORMATION
STN FORMAT: JP 1999-6108 19990113
ORIGINAL: JP11006108 Heisei
PRIORITY APPLN. INFO.: JP 1999-6108 19990113
SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
INT. PATENT CLASSIF.:
MAIN: H01L021-3205
ABSTRACT:

PROBLEM TO BE SOLVED: To suppress **diffusion** of **copper** atoms and to prevent peeling in the interface of a **copper** film and a first conductive film by using a material whose difference of a grating constant with **copper** is small as a first conductor film material.
SOLUTION: An insulating film 13 formed of a silicon oxide film and the like is formed on a whole face at the upper part of a MOS transistor. A plug formed of a main conductor film 15 **coating** adjacent conductor films 14a and 14b being first conductor films for **diffusion** prevention is formed in a contact hole formed in the insulating film 13 and it is connected to **diffusion layers** 2-5. When a **copper** film is used as the main conductor film 15, the adjacent conductor films 14a and 14b use one type among rhodium, **ruthenium**, iridium, osmium or white gold, whose lattice constant with the **copper** film is small, as a material. Thus, peeling at an interface between the **copper** film and the adjacent conductor films 14a and 14b can be prevented.

L41 ANSWER 5 OF 39 JAPIO (C) 2006 JPO on STN
ACCESSION NUMBER: 1999-317455 JAPIO
TITLE: **SEMICONDUCTOR** DEVICE AND ITS MANUFACTURE
INVENTOR: IWASAKI TOMIO; MIURA HIDEO
PATENT ASSIGNEE(S): HITACHI LTD
PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 11317455	A	19991116	Heisei	H01L021-768

APPLICATION INFORMATION
STN FORMAT: JP 1999-36824 19990216
ORIGINAL: JP11036824 Heisei
PRIORITY APPLN. INFO.: JP 1998-39992 19980223
SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
INT. PATENT CLASSIF.:
MAIN: H01L021-768
SECONDARY: H01L021-28
ABSTRACT:

PROBLEM TO BE SOLVED: To obtain a highly reliable **semiconductor** device, in which voids and disconnection are hard to occur by forming a **barrier** metal which is formed in contact with **copper** -film wiring of a **ruthenium** film and **copper** wiring in a laminated structure of a sputtered **copper** film and a plate **copper** film.
SOLUTION: In a laminated structure 6 composed of a conductive film 4 and an adjacent film 5 laminated upon the film 4 cove in contact with the film 4, the materials of the films 4 and 5 are selected so that the difference, {|a<SB>p</SB>-a<SB>n</SB>|/a<SB>p</SB>}×100=A (%), between the short side a<SB>p</SB> of the rectangular lattice constituting the minimum free energy surface of the conductive film 4 and the short side a<SB>n</SB> of the rectangular lattice constituting the minimum free energy surface of the adjacent film 5, and the difference between {|b<SB>p</SB>-b<SB>n</SB>|/b<SB>p</SB>}×100=B (%) between the long side b<SB>p</SB> of the rectangular lattice constituting the minimum free energy surface of the film 4 and the long side b<SB>n</SB> of the rectangular lattice constituting the minimum free energy surface of the film 5 satisfies the inequality, {A+B(a<SB>p</SB>/b<SB>p</SB>)<13.

L41 ANSWER 10 OF 39 JAPIO (C) 2006 JPO on STN
ACCESSION NUMBER: 1998-199970 JAPIO
TITLE: MANUFACTURE OF **SEMICONDUCTOR** ELEMENTS
INVENTOR: SAI GYOKON; BOKU KORAKU
PATENT ASSIGNEE(S): HYUNDAI ELECTRON IND CO LTD
PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 10199970	A	19980731	Heisei	H01L021-768

APPLICATION INFORMATION
STN FORMAT: JP 1996-351619 19961227
ORIGINAL: JP08351619 Heisei
PRIORITY APPLN. INFO.: JP 1996-351619 19961227
SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1998
INT. PATENT CLASSIF.:
MAIN: H01L021-768
ABSTRACT:

PROBLEM TO BE SOLVED: To avoid contacting a low-resistance **layer** to a dielectric film by etching an **Ru** nitride film and first metal **layer**, forming a W film on the side wall of the first metal **layer**, and connecting a second metal **layer** to the first metal **layer** through contact holes.
SOLUTION: A first **Cu layer** 32a is formed on a **semiconductor** substrate 31, and an **Ru** oxide film 33a is formed on the **Cu layer** 32a. Using a metal wiring mask, the oxide film 33a and **Cu layer** 32a are etched, and a W film 34 is formed selectively on the side wall of the remaining **Cu layer** 32a. To planarize the **layer** surface of the surface top of the entire structure, an insulation oxide film 35 easy to flow is formed and selectively removed to form contact holes for exposing the first **Cu layer** 32a, and a second metallic **layer** 37 is formed of Al, W, **Cu**, etc.

L41 ANSWER 15 OF 39 JAPIO (C) 2006 JPO on STN
ACCESSION NUMBER: 1997-213695 JAPIO
TITLE: **SEMICONDUCTOR** DEVICE AND MANUFACTURE THEREOF
INVENTOR: OOSAKO NAGISA
PATENT ASSIGNEE(S): FUJITSU LTD
PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 09213695	A	19970815	Heisei	H01L021-3205

APPLICATION INFORMATION
STN FORMAT: JP 1996-16797 19960201
ORIGINAL: JP08016797 Heisei
PRIORITY APPLN. INFO.: JP 1996-16797 19960201
SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1997
INT. PATENT CLASSIF.:
MAIN: H01L021-3205
ABSTRACT:

PROBLEM TO BE SOLVED: To form each antioxidation preventive film on the surfaces of **Cu** wirings and to prevent the **Cu** wirings from being oxidized by a method wherein a substrate is heat-treated and impurities being contained in the wirings are deposited on the surfaces of the wirings.
SOLUTION: A heat treatment of a substrate is performed in an Ar gas atmospohere. **Ru** atoms being contained in wirings 64a and 64b are deposited on the surfaces of the wirings 64a and 64b by this heat treatment and **protective** films 65a and 65b consisting of an **Ru** film are respectively formed on the surfaces of the wirings 64a and 64b. By depositing impurities being contained in the wirings on the surfaces of the wirings, the exposed surfaces of the wirings can be selectively **coated** with the films 65a and 65b. As the **Ru** film is oxidized more easily than a **Cu** film and is preferentially oxidized, an oxidation of the **Cu** wirings can be inhibited.

L41 ANSWER 38 OF 39 JAPIO (C) 2006 JPO on STN
ACCESSION NUMBER: 1980-070056 JAPIO
TITLE: PREPARATION OF THICK FILM HYBRID **INTEGRATED CIRCUIT**
INVENTOR: OTSU HIROSHI; ISOMAE HIROMI
PATENT ASSIGNEE(S): HITACHI LTD
PATENT INFORMATION:

PATENT NO	KIND	DATE	ERA	MAIN IPC
JP 55070056	A	19800527	Showa	H01L027-01

APPLICATION INFORMATION
STN FORMAT: JP 1978-143429 19781122
ORIGINAL: JP53143429 Showa
PRIORITY APPLN. INFO.: JP 1978-143429 19781122
SOURCE: PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1980
INT. PATENT CLASSIF.:
MAIN: H01L027-01
SECONDARY: H05K001-16; H05K003-46
ABSTRACT:

PURPOSE: To lower the resistance of conductor portions while eliminating solder encroaching properties, by forming multilayer wiring and circuit elements by means of printing, by **coating** a circuit element portion with glass, etc. and by plating the upper portions of conductor portions with **copper** by soaking a substrate in a chemical plating liquid.
CONSTITUTION: Circuit elements, such as, a resistor 5, etc. are made up in such a manner that a lower conductor 2, an insulator 3 and an upper conductor 4 are built up on an insulating substrate 1 in alumina, etc. by means of the printing and baking of Ag-Pd paste and borosilicate lead glass, and **ruthenium** oxide resistance paste, etc. are printed and baked. A circuit element 5 portion is **coated** with glass or resin 7, and the portions, which are not covered with insulators 7, 3, of the upper conductor 4 and the lower conductor 2 are plated with **copper** 8 by immersing the substrate 1 in a chemical **copper** plating liquid. Thus, the **impedance** of the conductor portions 2, 4 is lowered while solder encroaching properties are eliminated, solder moistening properties are bettered, the connection of parts by means of soldering is made possible and an integrating degree can be improved.